integrated circuit chip connected via a peripheral bus to a secondary processor on a second integrated circuit chip, the method comprising the steps of:

decompressing at least a system layer, which is a higher level layer than a video layer, of the compressed data in the host processor; and

decompressing other data layers of the set including the video layer in the secondary processor.

2. The method of Claim 1, wherein the secondary processor is a graphics accelerator.

3. (Amended) The method of Claim 1, wherein the secondary processor is a dedicated MPEG decompression circuit for decompression of data subject to MPEG compression and the host processor is a general purpose microprocessor.

4. The method of Claim 1, wherein the step of decompressing at least a system layer further comprises decompressing a book layer of the set.

5. The method of Claim 1, wherein the data includes audio and video data.

6. The method of Claim 1, wherein the step of decompressing other data layers includes the steps of:

variable length decoding the compressed data;

inverse zig-zagging the decoded data;

inverse quantizing the zig-zagged data, and inverse discrete cosine transforming the inverse quantized data.

7. The method of Claim 1, wherein the step of decompressing other data layers includes motion vector compensation of the data.

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

8. (Amended) A computer system adapted for decompression of compressed data which is in a set of predetermined data layers, comprising:

a host processor on a first integrated circuit chip;

a peripheral bus connected to the host processor;

a secondary processor on a second integrated circuit chip and connected to the peripheral bus; and

means for decompressing in the host processor at least a system layer, which is a higher level layer than a video layer, of the compressed data, wherein other data layers of the set including the video layer are decompressed in the secondary processor.

9. The system of Claim 8, wherein the secondary processor is a graphics accelerator.

10. (Amended) The system of Claim 8, wherein the secondary processor is a dedicated decompression circuit for decompression of data which has been compressed using MPEG compression and the host processor is a general purpose microprocessor.

11. The system of Claim 8, wherein the means for decompressing at least a system layer further comprises decompressing means for decompressing a book layer of the set.

12. The system of Claim 8, wherein the data includes audio and video data.

13. The system of Claim 8, wherein the means for decompressing at least the system layer includes:

means for variable length decoding the compressed data;

means for inverse zig-zagging the decoded data; and

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

means for inverse quantizing the data.

14. The system of Claim 8, wherein decompression of the other layers of the set includes motion vector compensation of the data.

15. The computer system of Claim 8, further comprising a frame buffer connected to the secondary processor.

REMARKS

Claims 1-15 were pending in the case and all stand rejected. Reconsideration is requested.

The amendments to the specification are to conform the specification to the drawings. The requested amendment to the drawing is to conform the drawing to the originally filed specification. The Examiner is thanked for the close attention paid to the specification and drawings.

Claims 1, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, and 15 stand rejected under 35 U.S.C. Section 103(a) as unpatentable over Purcell et al. in view of Normile et al. The Examiner stated in pertinent part:

> Purcell et al discloses all the claimed subject matter except a host processor and a peripheral bus connected to the host processor. However, Normile et al clearly discloses a host processor (Figure 4, #410) and a peripheral bus (i.e., Bus, Figure 4, #425) connected to the host processor. The host processor taught by Normile et al processes at least a system layer of compressed data. That is, the host processor reads and determines one complete frame of compressed date from a disk or memory and transfers the data to the coprocessors ...

Claims 2 and 9 stand rejected under 35 U.S.C. Section 103(a) as unpatentable over Purcell et al. and Normile et al. and further in view of Harney et al.

The claims have been amended, and it is respectfully submitted that the claims distinguish over the references, even in combination, for the reasons set forth below. Therefore, it

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979